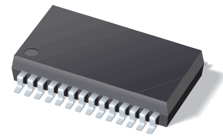


STEREO AUDIO CODEC WITH USB INTERFACE, SINGLE-ENDED ANALOG INPUT/OUTPUT AND S/PDIF

FEATURES

- **PCM2900: Without S/PDIF**
- **PCM2902: With S/PDIF**
- **On-Chip USB Interface:**
  - **With Full-Speed Transceivers**
  - **Fully Compliant With USB 1.1 Specification**
  - **Certified by USB-IF**
  - **Partially Programmable Descriptors** (1)
  - **USB Adaptive Mode for Playback**
  - **USB Asynchronous Mode for Record**
  - **Bus Powered**
- **16-Bit Delta-Sigma ADC and DAC**
- **Sampling Rate:**
  - **DAC: 32, 44.1, 48 kHz**
  - **ADC: 8, 11.025, 16, 22.05, 32, 44.1, 48 kHz**
- **On-Chip Clock Generator With Single 12-MHz Clock Source**
- **Single Power Supply: 5 V Typical (V_{BUS})**
- **Stereo ADC**
  - **Analog Performance at V_{BUS} = 5 V**
    - **THD+N = 0.01%**
    - **SNR = 89 dB**
    - **Dynamic Range = 89 dB**
  - **Decimation Digital Filter**
    - **Pass-Band Ripple = ±0.05 dB**
    - **Stop-Band Attenuation = 65 dB**
  - **Single-Ended Voltage Input**
  - **Antialiasing Filter Included**
  - **Digital LCF Included**
- **Stereo DAC**
  - **Analog Performance at V_{BUS} = 5 V**
    - **THD+N = 0.005%**
    - **SNR = 96 dB**
    - **Dynamic Range = 93 dB**
  - **Oversampling Digital Filter**
    - **Pass-Band Ripple = ±0.1 dB**
    - **Stop-Band Attenuation = –43 dB**
  - **Single-Ended Voltage Output**
  - **Analog LPF Included**
- **Multifunctions:**
  - **Human Interface Device (HID) Volume ± Control and Mute Control**
  - **Suspend Flag**
- **Package: 28-Pin SSOP**

(1) The descriptor can be modified by changing a mask.

APPLICATIONS

- **USB Audio Speaker**
- **USB Headset**
- **USB Monitor**
- **USB Audio Interface Box**

DESCRIPTION

The PCM2900/2902 is Texas Instruments' single-chip USB stereo audio codec with USB-compliant full-speed protocol controller and S/PDIF (only PCM2902). The USB protocol controller works with no software code, but the USB descriptors can be modified in some areas (e.g., vendor ID/product ID). The PCM2900/2902 employs SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog PLLs with SpAct architecture enable playback and record with low clock jitter and with independent playback and record sampling rates.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING ORDERING INFORMATION

PCM2900						
PRODUCT	**PACKAGE-LEAD**	**PACKAGE DESIGNATOR**	**SPECIFIED TEMPERATURE RANGE**	**PACKAGE MARKING**	**ORDERING NUMBER**(1)	**TRANSPORT MEDIA**
PCM2900E	SSOP-28	28DB	–25°C to 85°C	PCM2900E	PCM2900E	Rails
					PCM2900E/2K	Tape and reel

(1) Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM2900E/2K gets a single 2000-piece tape and reel.

PCM2902						
PRODUCT	**PACKAGE-LEAD**	**PACKAGE DESIGNATOR**	**SPECIFIED TEMPERATURE RANGE**	**PACKAGE MARKING**	**ORDERING NUMBER**(1)	**TRANSPORT MEDIA**
PCM2902E	SSOP-28	28DB	–25°C to 85°C	PCM2902E	PCM2902E	Rails
					PCM2902E/2K	Tape and reel

(1) Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM2902E/2K gets a single 2000-piece tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			PCM2900/PCM2902	UNIT
V_{BUS}	Supply voltage		–0.3 to 6.5	V
	Ground voltage differences, AGNDC, AGNDP, AGNDX, DGND, DGNDU		±0.1	V
	Digital input voltage	SEL0, SEL1, TEST0 (DIN)(2)	–0.3 to 6.5	V
		D+, D–, HID0, HID1, HID2, XTI, XTO, TEST1 (DOUT)(2), $\overline{\text{SSPND}}$	–0.3 to (V_{DDI} + 0.3) < 4	V
	Analog input voltage	$V_{IN}L$, $V_{IN}R$, V_{COM}, $V_{OUT}R$, $V_{OUT}L$	–0.3 to (V_{CCCI} + 0.3) < 4	V
		V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, V_{DDI}	–0.3 to 4	V
	Input current (any pins except supplies)		±10	mA
	Ambient temperature under bias		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	°C
T_J	Junction temperature		150	°C
	Lead temperature (soldering)		260	°C, 5 s
	Package temperature (IR reflow, peak)		250	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ( ): PCM2902

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER			TEST CONDITIONS	PCM2900E, PCM2902E			UNIT
				MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT							
	Host interface		Apply USB Revision 1.1, full speed				
	Audio data format		USB isochronous data format				
INPUT LOGIC							
V_{IH}	High-level input voltage	D+, D–		2		3.3	VDC
		XTI, HID0, HID1, and HID2		2.52		3.3	
		SEL0, SEL1		2		5.25	
		DIN, PCM2902		2.52		5.25	
V_{IL}	Low-level input voltage	D+, D–				0.8	VDC
		XTI, HID0, HID1, and HID2				0.9	
		SEL0, SEL1				0.8	
		DIN, PCM2902				0.9	
I_{IH}	High-level input voltage	D+, D–, XTI, SEL0, SEL1	V_{IN} = 3.3 V			±10	μA
		HID0, HID1, and HID2			50	80	
		DIN, PCM2902			65	100	
I_{IL}	Low-level input voltage	D+, D–, XTI, SEL0, SEL1	V_{IN} = 0 V			±10	μA
		HID0, HID1, and HID2				±10	
		DIN, PCM2902				±10	
OUTPUT LOGIC							
V_{OH}	High-level output voltage	D+, D–		2.8			VDC
		DOUT, PCM2902	I_{OH} = –4 mA	2.8			
		$\overline{\text{SSPND}}$	I_{OH} = –2 mA	2.8			
V_{OL}	Low-level output voltage	D+, D–				0.3	VDC
		DOUT, PCM2902	I_{OL} = 4 mA			0.5	
		$\overline{\text{SSPND}}$	I_{OL} = 2 mA			0.5	
CLOCK FREQUENCY							
	Input clock frequency, XTI			11.994	12	12.008	MHz
ADC CHARACTERISTICS							
	Resolution				8, 16		bits
	Audio data channel				1, 2		channel

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM2900E, PCM2902E			UNIT
			MIN	TYP	MAX	
CLOCK FREQUENCY						
f_S	Sampling frequency		8, 11.025, 16, 22.05, 32, 44.1, 48			kHz
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±0		% of FSR
DYNAMIC PERFORMANCE(1)						
THD+N	Total harmonic distortion plus noise	V_{CCCI} = 3.67 V, V_{IN} = –0.5 dB(2)		0.01%	0.02%	
		V_{IN} = –0.5 dB(3)		0.1%		
		V_{IN} = –60 dB		5%		
	Dynamic range	A-weighted	81	89		dB
SNR	Signal-to-noise ratio	A-weighted	81	89		dB
	Channel separation		80	85		dB
ANALOG INPUT						
	Input voltage			0.6 V_{CCCI}		V_{p-p}
	Center voltage			0.5 V_{CCCI}		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		65			dB
t_d	Delay time			17.4/f_S		s
	LCF frequency response	–3 dB		0.078 f_S		MHz
DAC CHARACTERISTICS						
	Resolution			8, 16		bits
	Audio data channel			1, 2		channel
CLOCK FREQUENCY						
f_S	Sampling frequency			32, 44.1, 48		kHz

(1) f_{IN} = 1 kHz, using a System Two™ audio measurement system by Audio Precision™ in the RMS mode with 20-kHz LPF, 400-Hz HPF in calculation.
(2) Using external voltage regulator for V_{CCCI} (as shown in Figure 36 and Figure 37, using with REG103xA-A)
(3) Using internal voltage regulator for V_{CCCI} (as shown in Figure 38 and Figure 39)

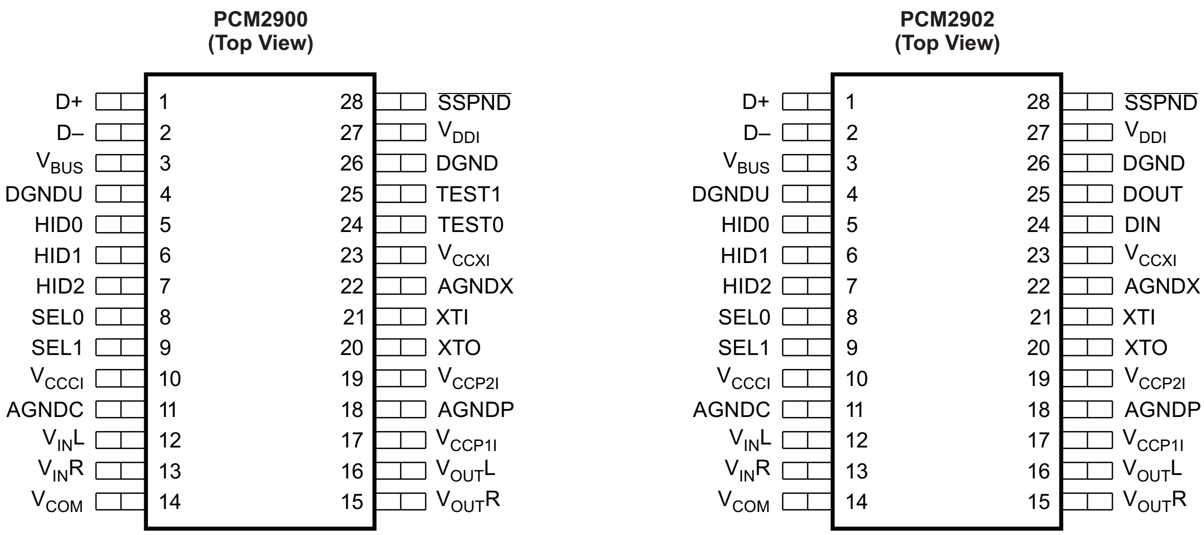
ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER			TEST CONDITIONS	PCM2900E, PCM2902E			UNIT
				MIN	TYP	MAX	
DC ACCURACY							
	Gain mismatch channel-to-channel				±1	±5	% of FSR
	Gain error				±2	±10	% of FSR
	Bipolar zero error				±2		% of FSR
DYNAMIC PERFORMANCE (1)							
THD+N	Total harmonic distortion plus noise		V_{OUT} = 0 dB		0.005%	0.016%	
			V_{OUT} = –60 dB		3%		
	Dynamic range		EIAJ, A-weighted	87	93		dB
SNR	Signal-to-noise ratio		EIAJ, A-weighted	90	96		dB
	Channel separation			86	92		dB
ANALOG OUTPUT							
V_O	Output voltage				0.6 V_{CCCI}		V_{p-p}
	Center voltage				0.5 V_{CCCI}		V
	Load impedance		AC coupling	10			kΩ
	LPF frequency response		–3 dB		250		kHz
			f = 20 kHz		–0.03		dB
	Digital filter performance						
	Pass band					0.445 f_S	Hz
	Stop band			0.555 f_S			Hz
	Pass-band ripple					±0.1	dB
	Stop-band attenuation			–43			dB
t_d	Delay time				14.3 f_S		s
POWER SUPPLY REQUIREMENTS							
V_{BUS}	Voltage range			4.35	5	5.25	VDC
	Supply current		ADC, DAC operation		56	67	mA
			Suspend mode (2)		210		µA
P_D	Power dissipation		ADC, DAC operation		280	352	mW
			Suspend mode (2)		1.05		mW
	Internal power supply voltage	V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, and V_{DDI}		3.25	3.35	3.5	VDC
TEMPERATURE RANGE							
	Operation temperature			–25		85	°C
θ_{JA}	Thermal resistance				100		°C/W

(1) f_{OUT} = 1 kHz, using a System Two audio measurement system by Audio Precision in the RMS mode with 20-kHz LPF, 400-Hz HPF.
(2) Under USB suspend state

PIN ASSIGNMENTS



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PCM2900 TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
HID0	5	I	HID key state input (mute), active-high(2)
HID1	6	I	HID key state input (volume up), active-high(2)
HID2	7	I	HID key state input (volume down), active-high(2)
SEL0	8	I	Must be set to high(3)
SEL1	9	I	Must be set to high(3)
$\overline{\text{SSPND}}$	28	O	Suspend flag, active-low (Low: suspend, High: operational)
TEST0	24	I	Test pin, must be connected to GND
TEST1	25	O	Test pin, must be left open
V_{BUS}	3	–	Connect to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(4)
V_{CCP1I}	17	–	Internal analog power supply for PLL(4)
V_{CCP2I}	19	–	Internal analog power supply for PLL(4)
V_{CCXI}	23	–	Internal analog power supply for oscillator(4)
V_{COM}	14	–	Common for ADC/DAC (V_{CCCI}/2)(4)
V_{DDI}	27	–	Internal digital power supply(4)
V_{IN}L	12	I	ADC analog input for L-channel
V_{IN}R	13	I	ADC analog input for R-channel
V_{OUT}L	16	O	DAC analog output for L-channel
V_{OUT}R	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input (5)
XTO	20	O	Crystal oscillator output

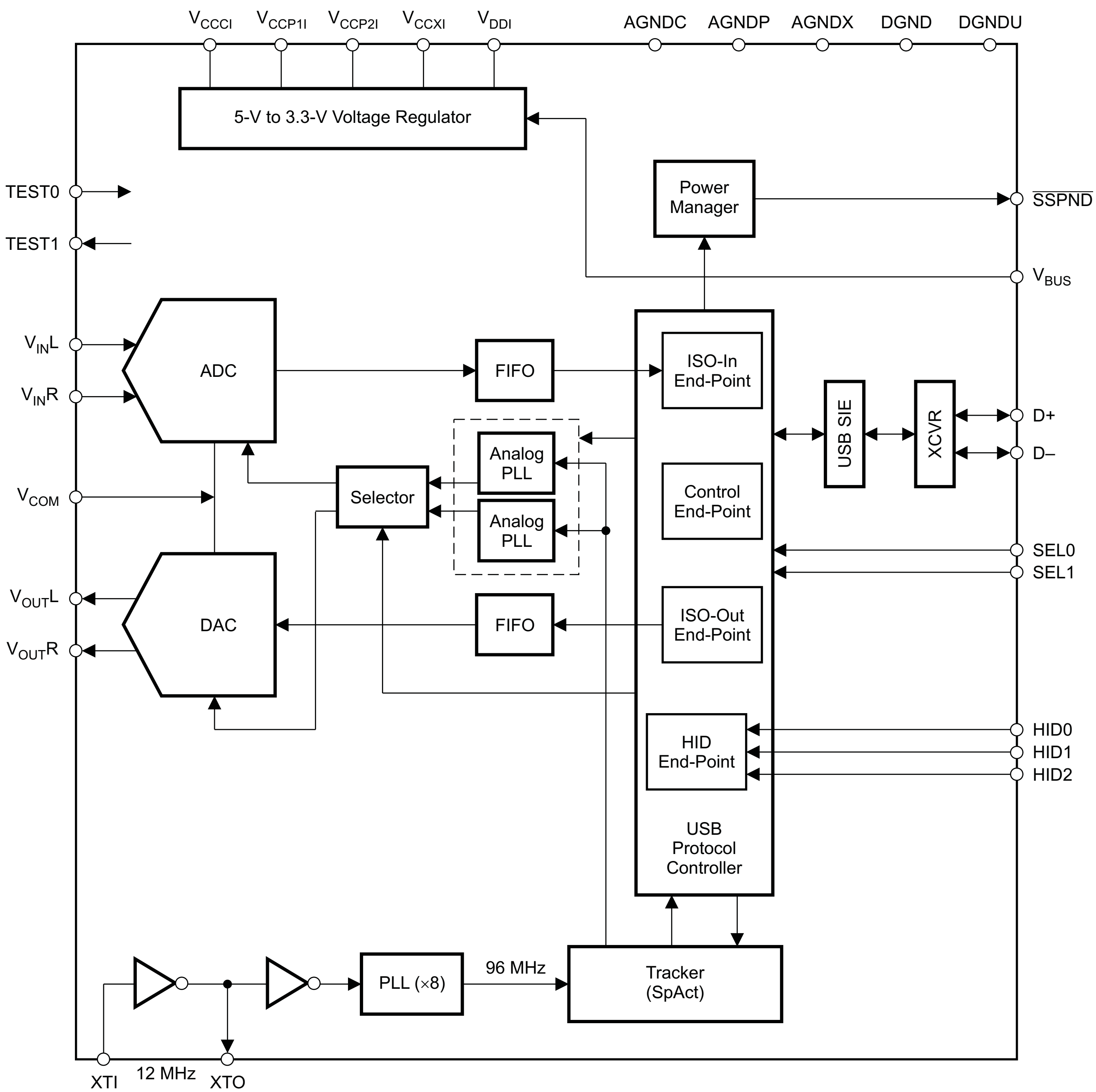
(1) LV-TTL level
(2) 3.3-V CMOS-level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no connection with the internal DAC or ADC directly. See the *Interface #3* and *End-Points* sections.
(3) TTL Schmitt trigger, 5-V tolerant
(4) Connect a decoupling capacitor to GND.
(5) 3.3-V CMOS-level input

PCM2902 TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
DIN	24	I	S/PDIF input(2)
DOUT	25	O	S/PDIF output
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(4)
SEL1	9	I	Must be set to high(4)
$\overline{\text{SSPND}}$	28	O	Suspend flag, active-low (Low: suspend, High: operational)
V_{BUS}	3	–	Connect to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(5)
V_{CCP1I}	17	–	Internal analog power supply for PLL(5)
V_{CCP2I}	19	–	Internal analog power supply for PLL(5)
V_{CCXI}	23	–	Internal analog power supply for oscillator(5)
V_{COM}	14	–	Common for ADC/DAC (V_{CCCI}/2)(5)
V_{DDI}	27	–	Internal digital power supply
V_{IN}L	12	I	ADC analog input for L-channel
V_{IN}R	13	I	ADC analog input for R-channel
V_{OUT}L	16	O	DAC analog output for L-channel
V_{OUT}R	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(6)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level
(2) 3.3-V CMOS-level input with internal pulldown, 5-V tolerant
(3) 3.3-V CMOS-level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no connection with the internal DAC or ADC directly. See the *Interface #3* and *End-Points* sections.
(4) TTL Schmitt trigger, 5-V tolerant
(5) Connect a decoupling capacitor to GND.
(6) 3.3-V CMOS-level input

PCM2900 FUNCTIONAL BLOCK DIAGRAM



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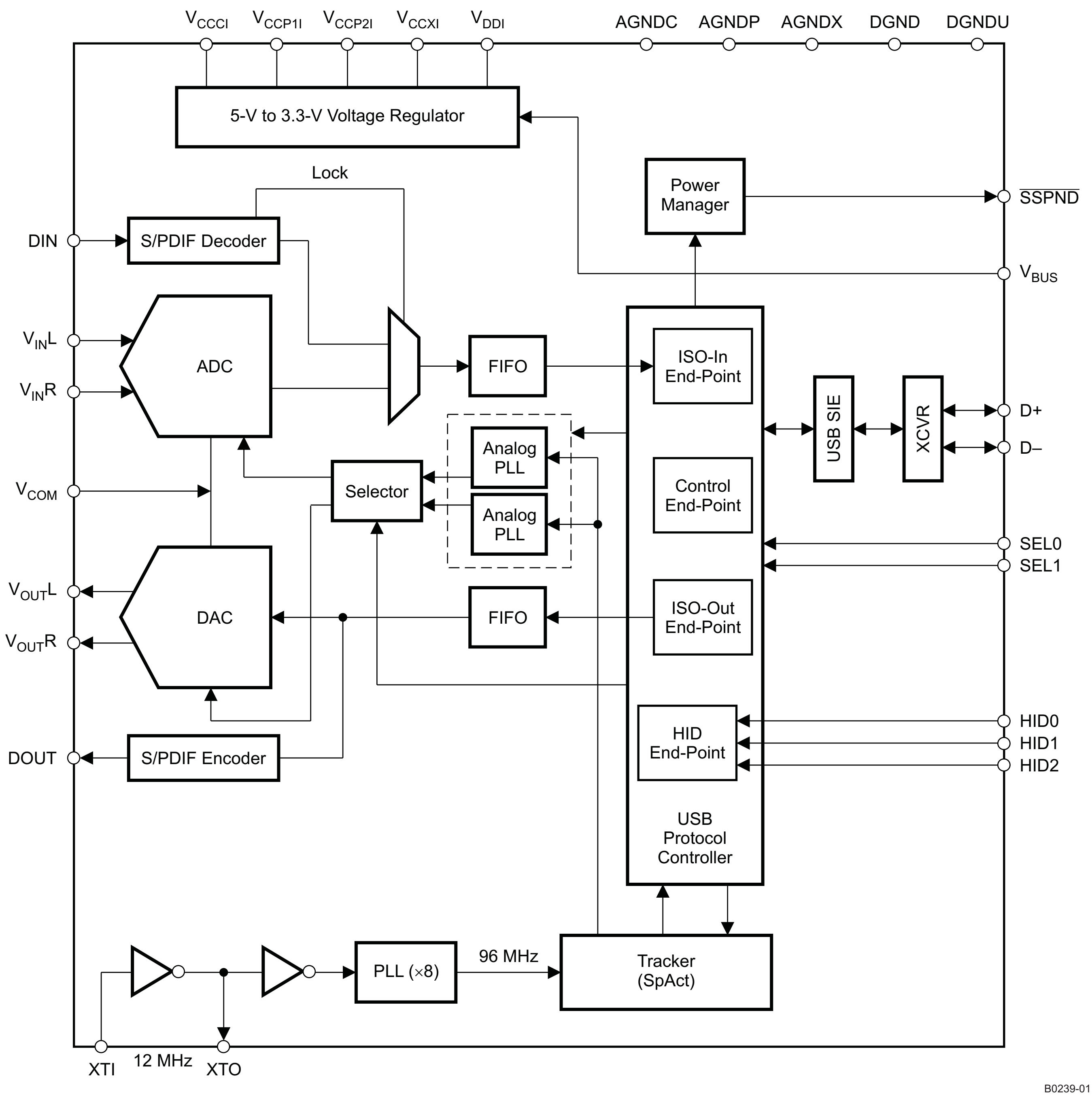
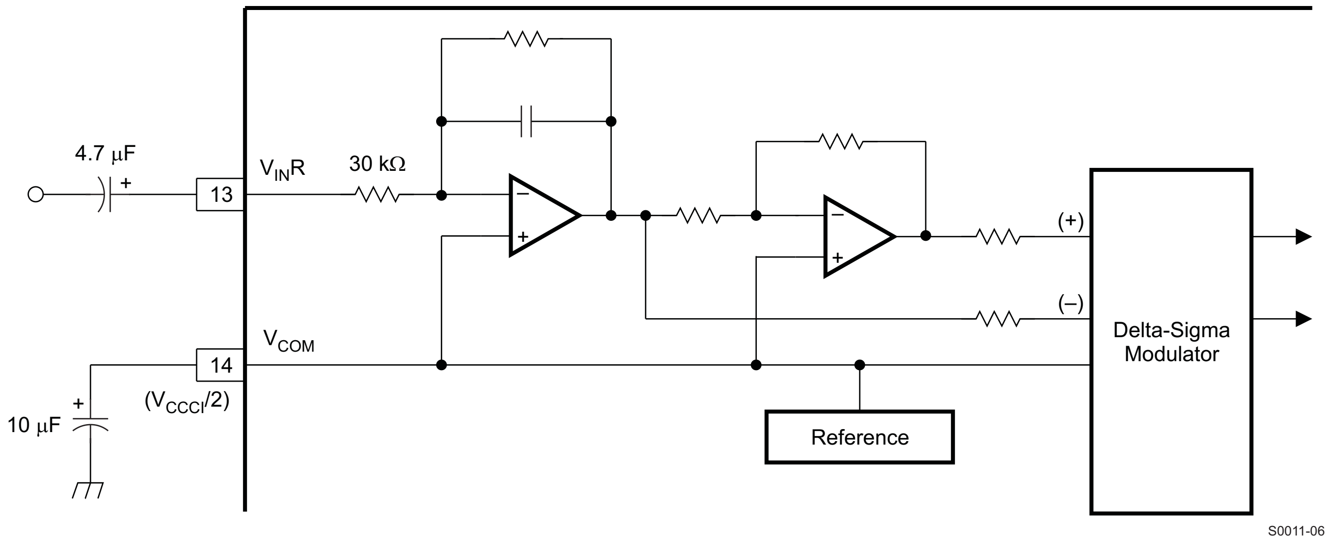
PCM2902 FUNCTIONAL BLOCK DIAGRAM



PCM2900/2902 DIAGRAM OF ANALOG FRONT-END (RIGHT CHANNEL)



TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted

ADC

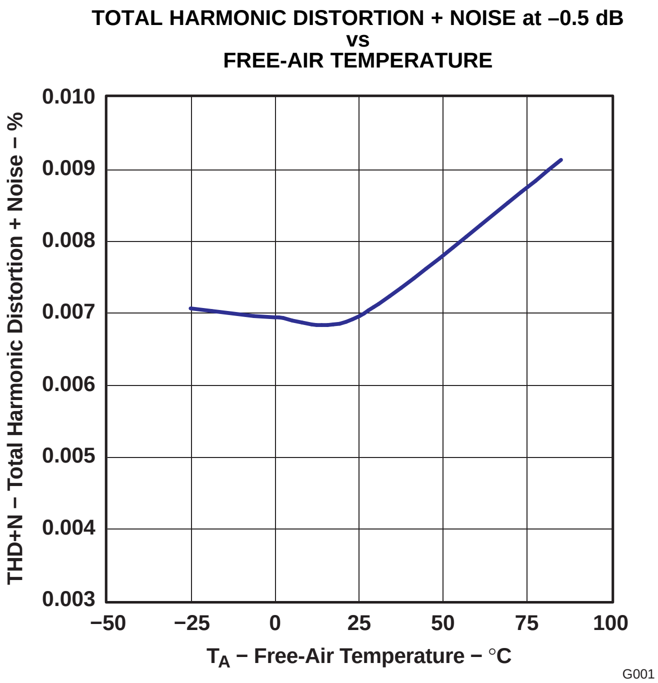


Figure 1.

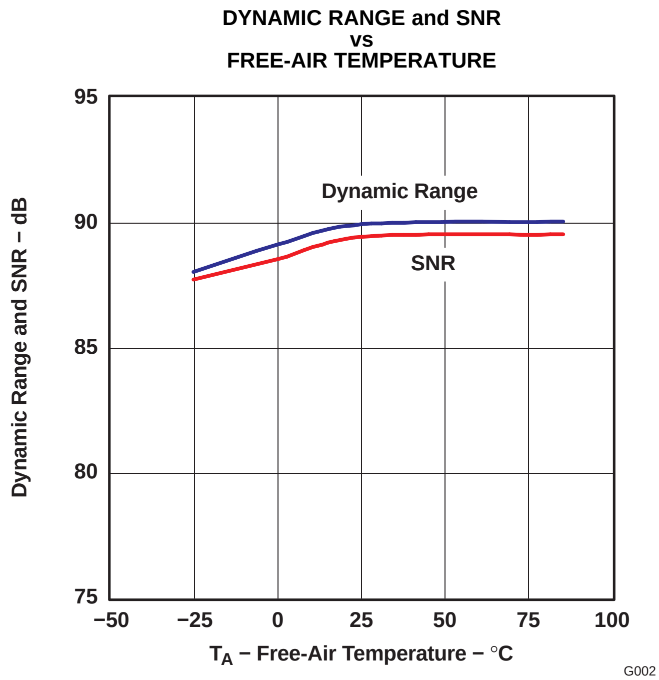


Figure 2.

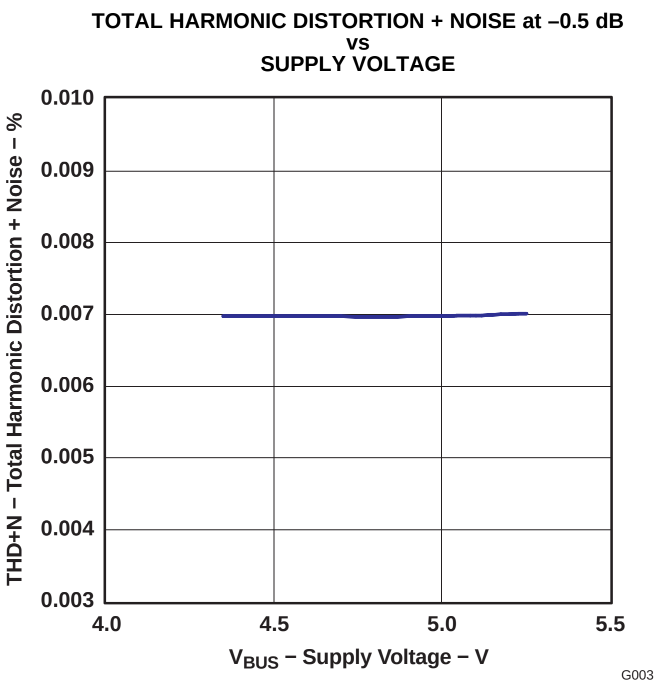


Figure 3.

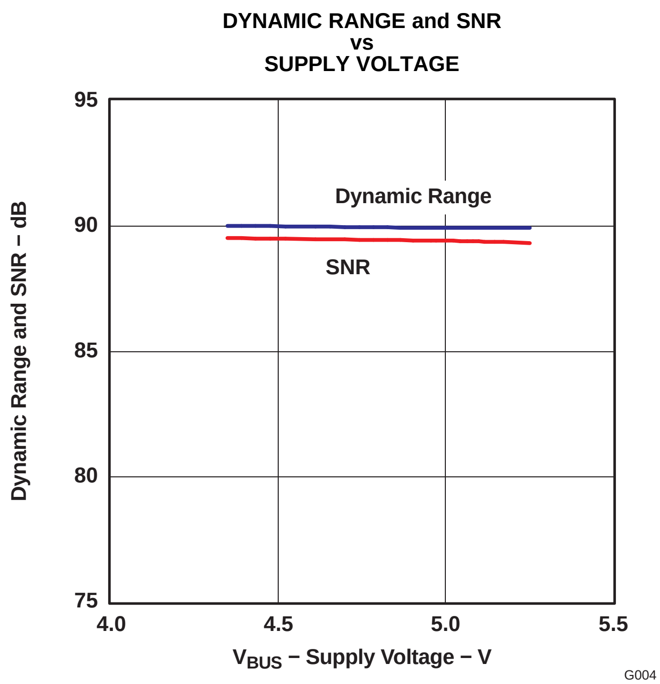


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted

TOTAL HARMONIC DISTORTION + NOISE at –0.5 dB vs SAMPLING FREQUENCY

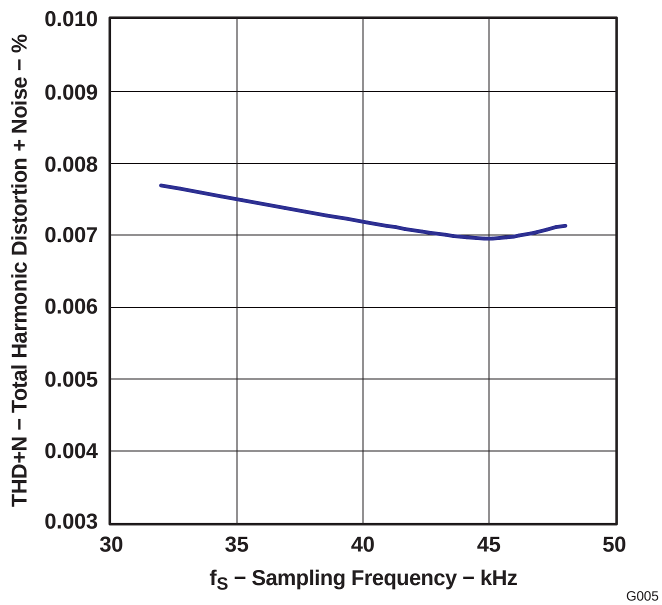


Figure 5.

DYNAMIC RANGE AND SNR vs SAMPLING FREQUENCY

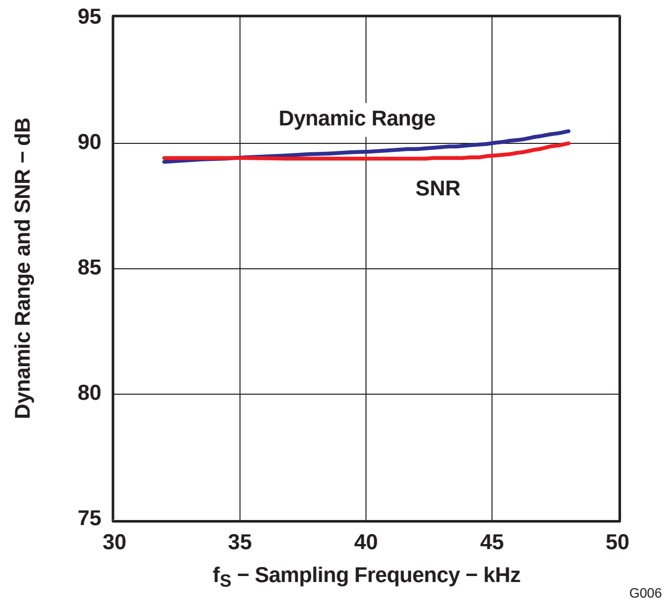


Figure 6.

DAC

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs FREE-AIR TEMPERATURE

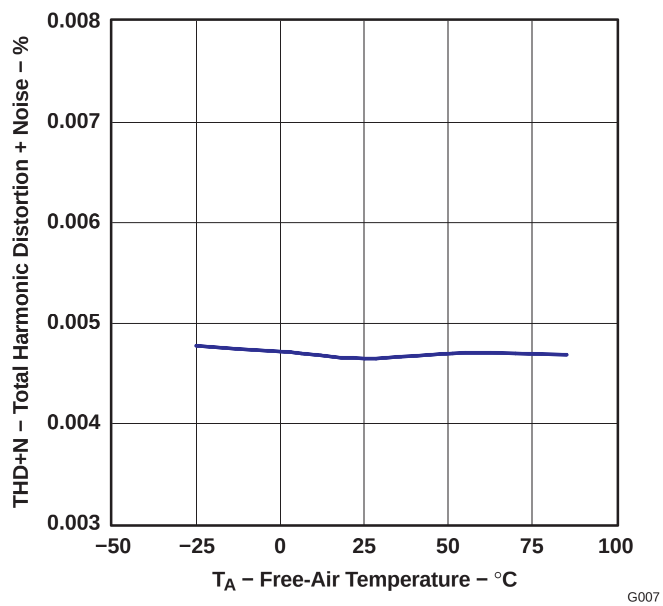


Figure 7.

DYNAMIC RANGE AND SNR vs FREE-AIR TEMPERATURE

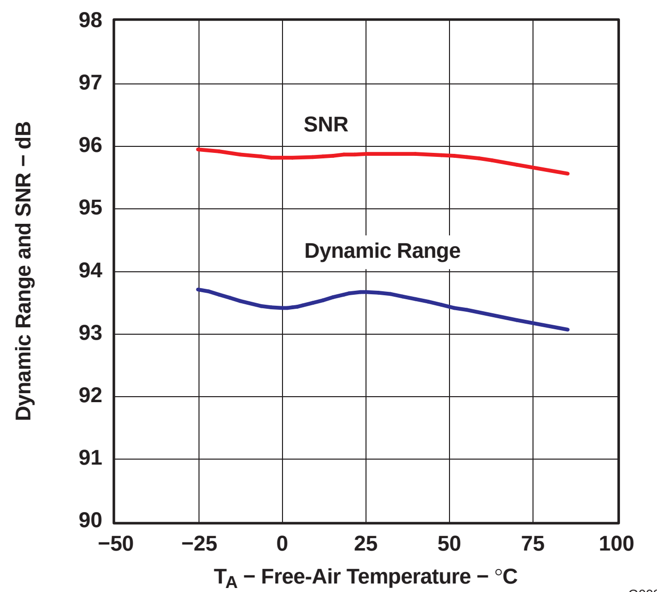


Figure 8.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted

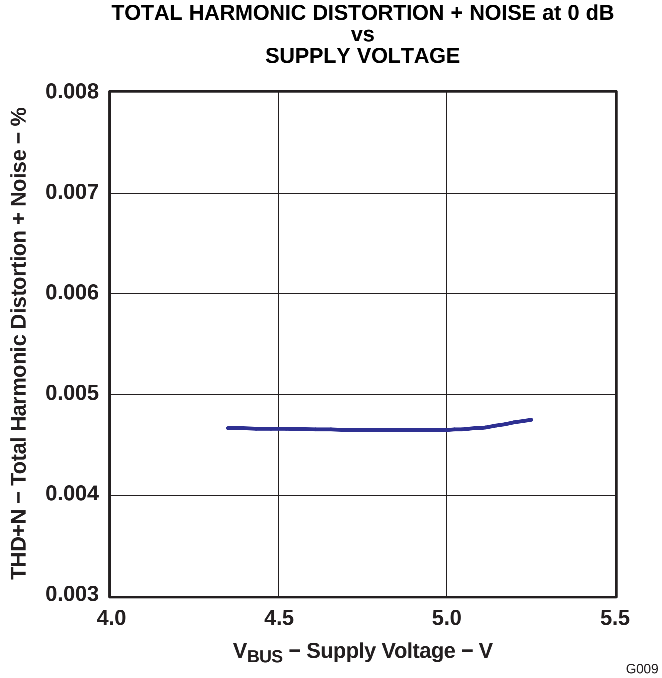


Figure 9.

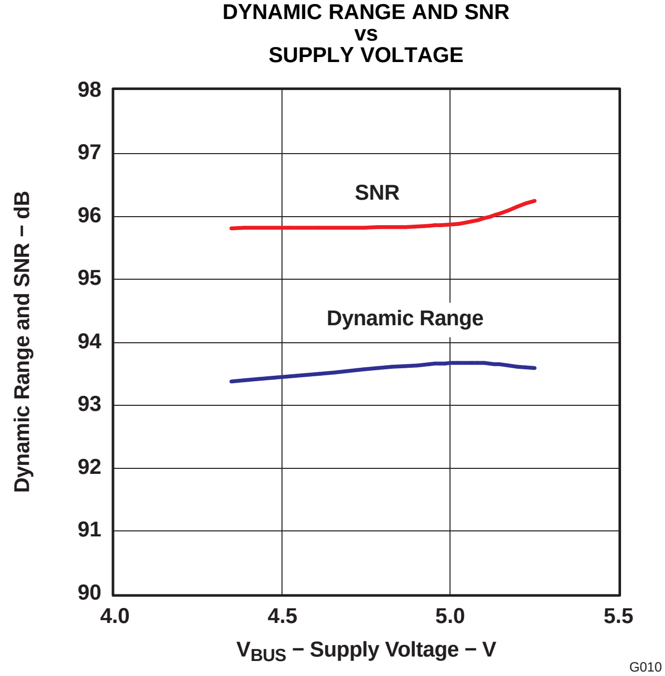


Figure 10.

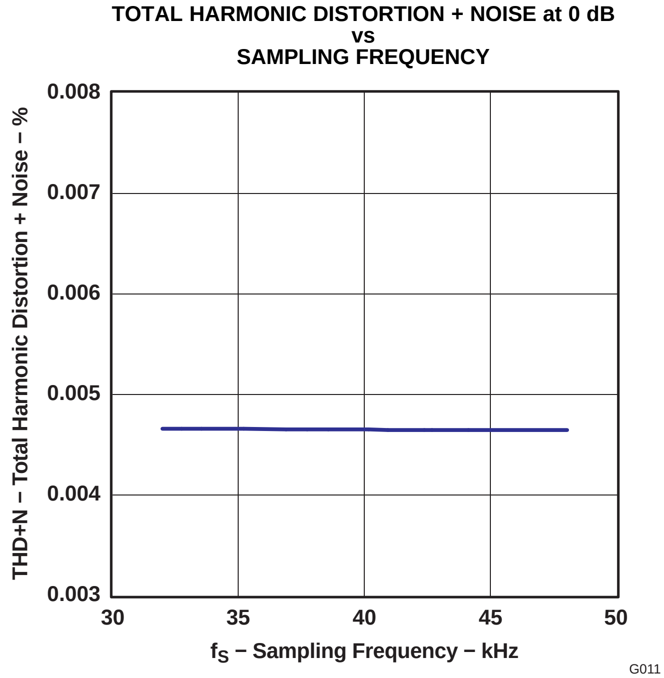


Figure 11.

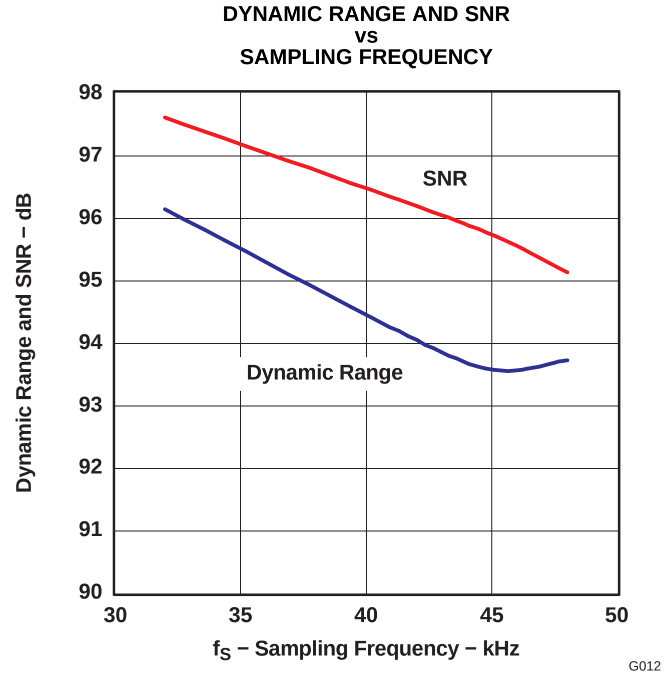


Figure 12.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted

SUPPLY CURRENT

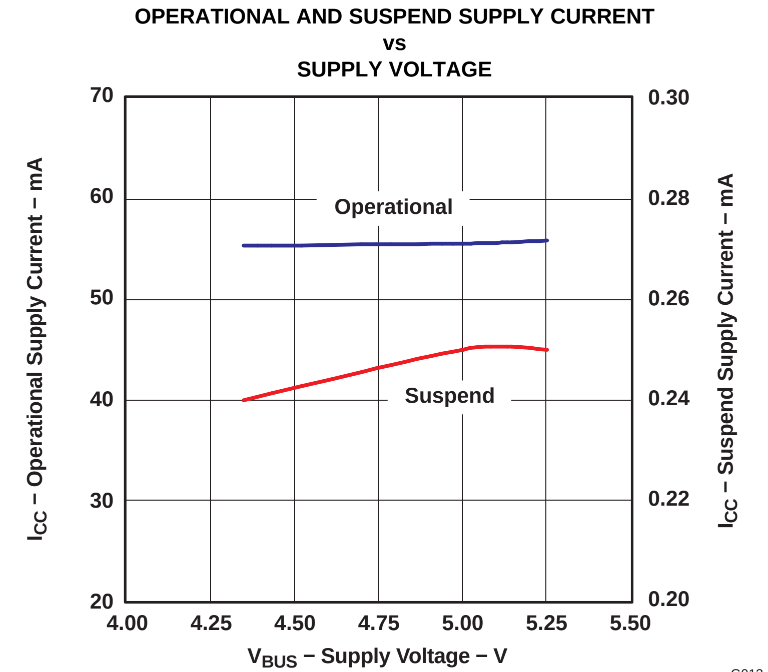


Figure 13.

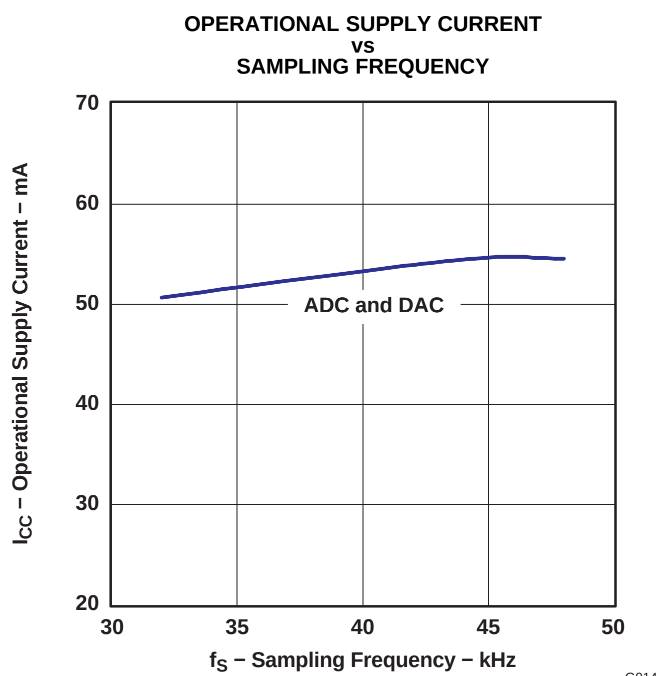


Figure 14.

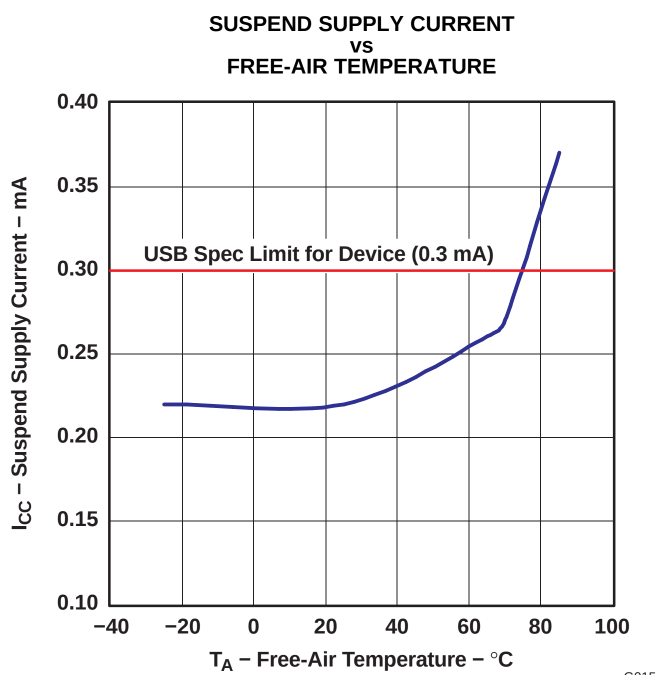


Figure 15.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted

ADC DIGITAL DECIMATION FILTER FREQUENCY RESPONSE

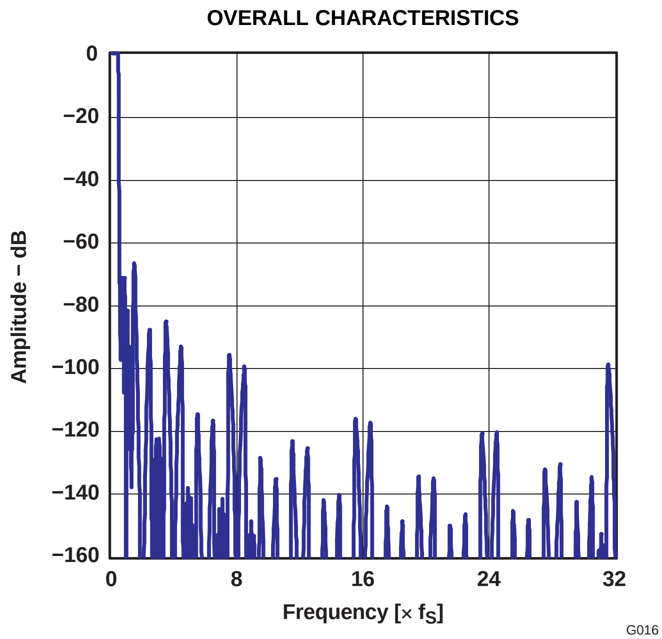


Figure 16.

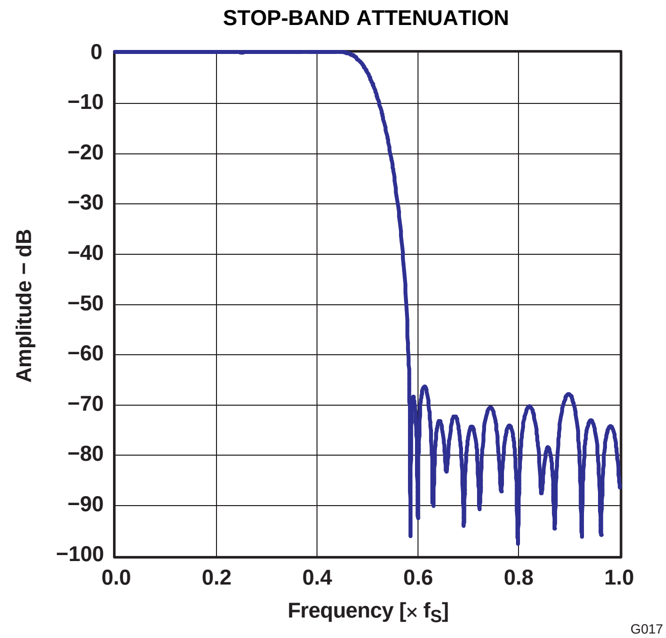


Figure 17.

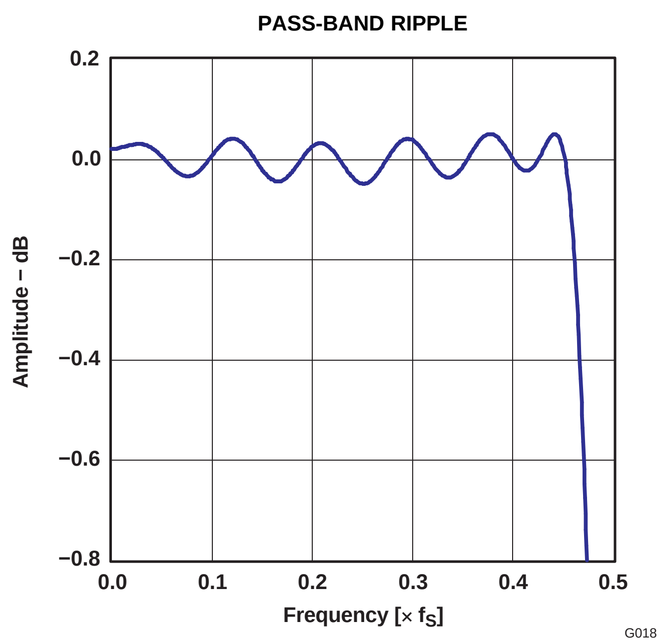


Figure 18.

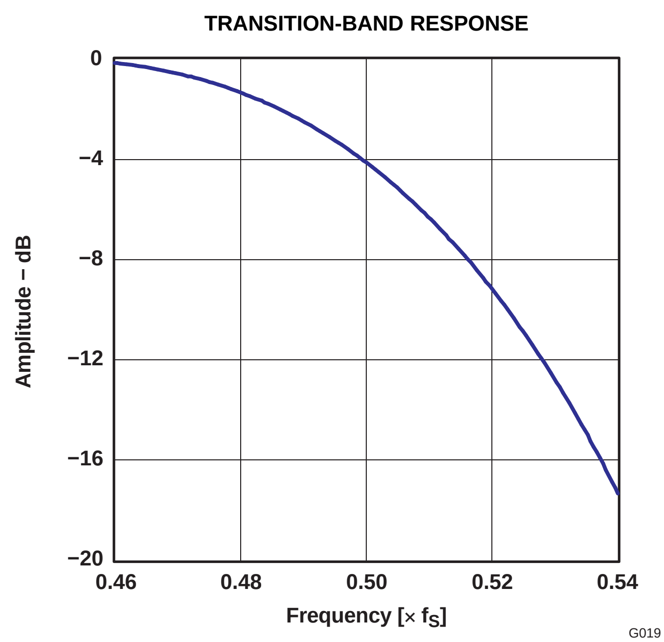


Figure 19.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted

ADC DIGITAL HIGH-PASS FILTER FREQUENCY RESPONSE

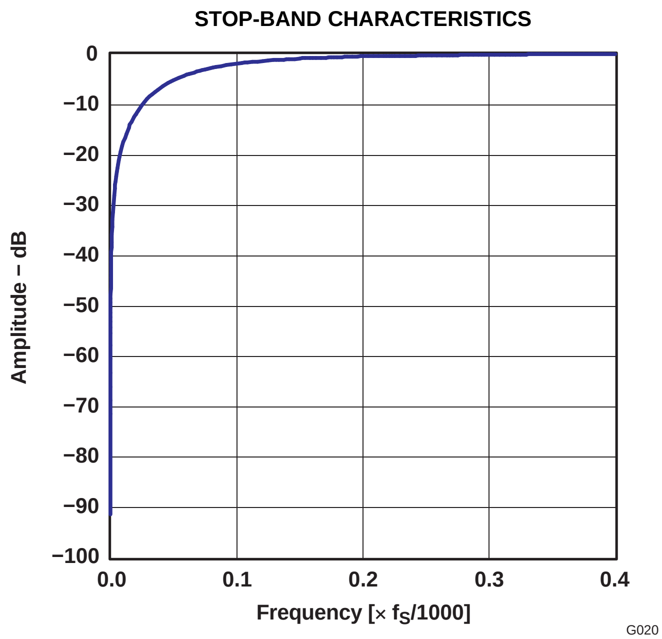


Figure 20.

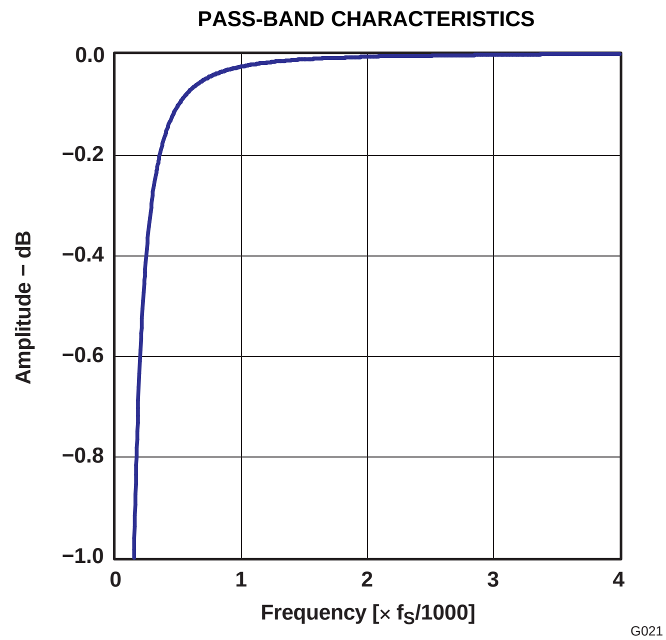


Figure 21.

ADC ANALOG ANTIALIASING FILTER FREQUENCY RESPONSE

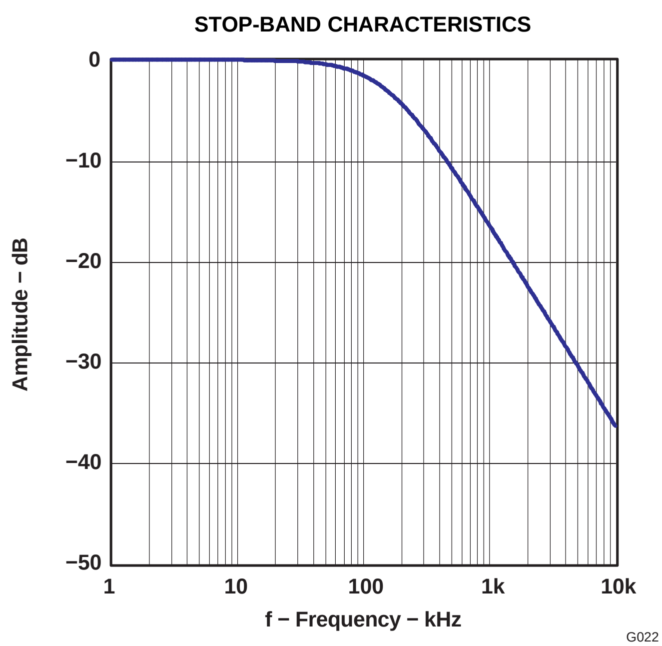


Figure 22.

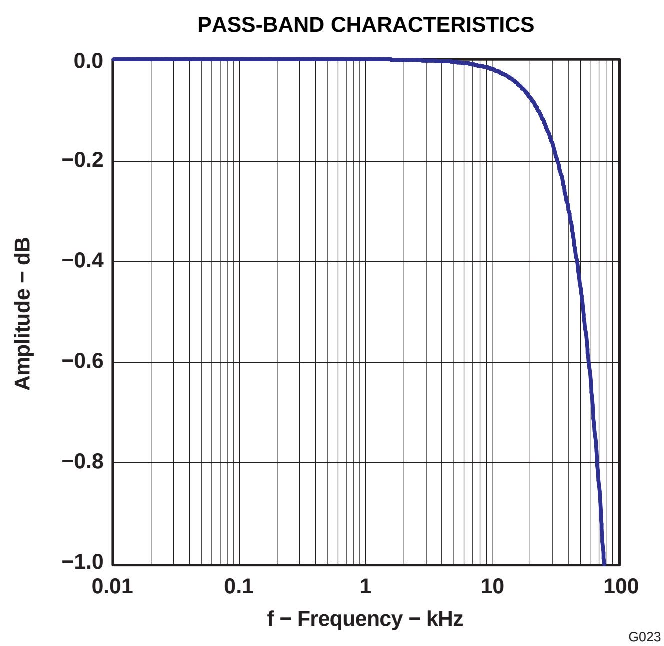


Figure 23.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted

DAC DIGITAL INTERPOLATION FILTER FREQUENCY RESPONSE

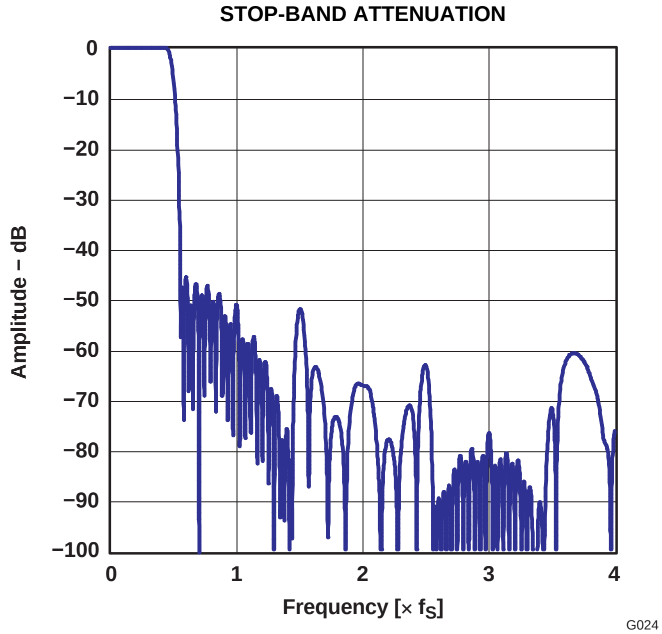


Figure 24.

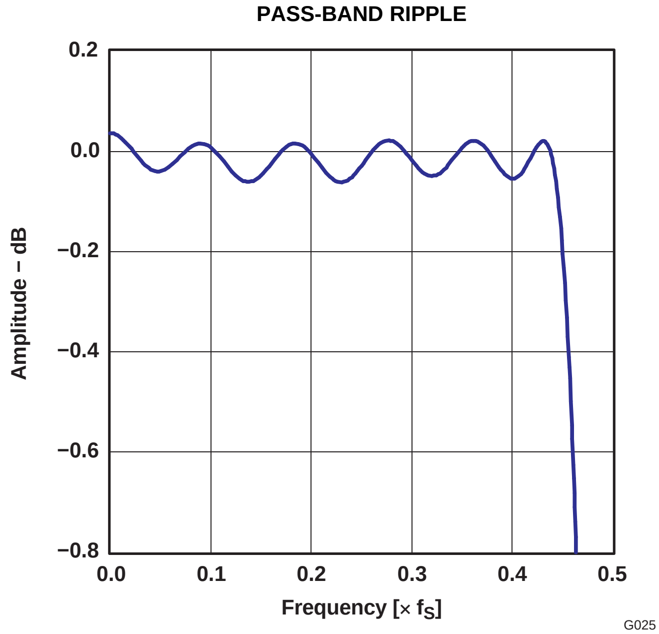


Figure 25.

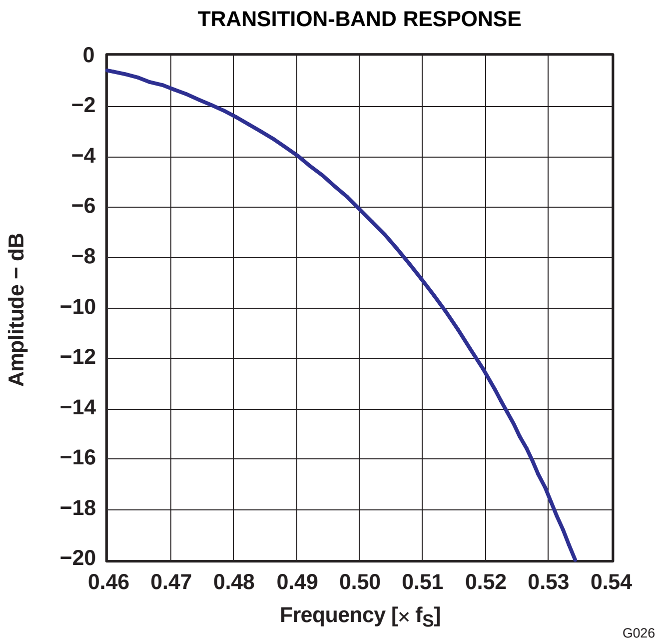


Figure 26.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted

DAC ANALOG FIR FILTER FREQUENCY RESPONSE

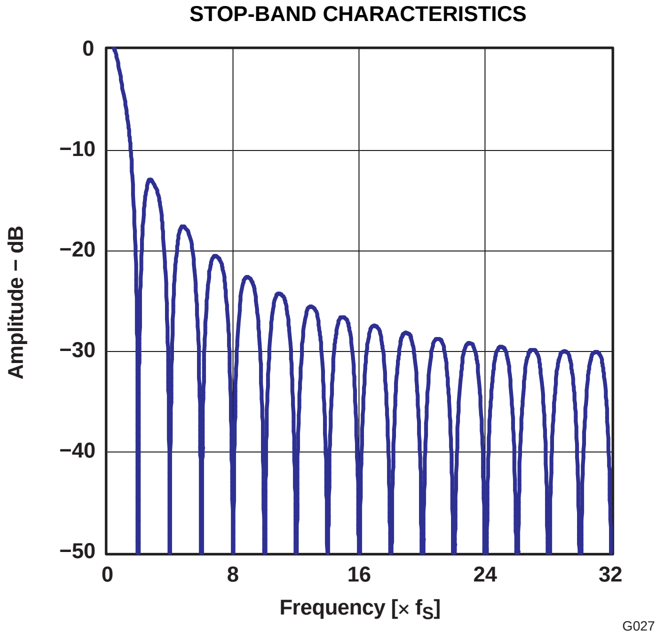


Figure 27.

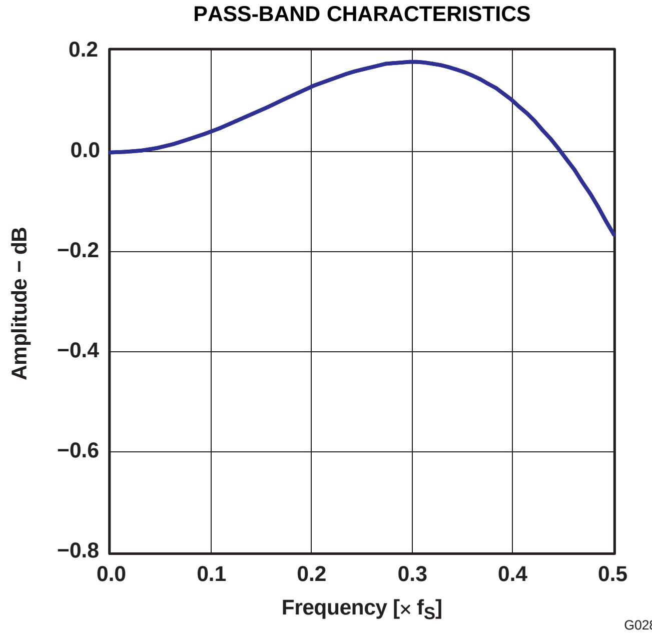


Figure 28.

DAC ANALOG LOW-PASS FILTER FREQUENCY RESPONSE

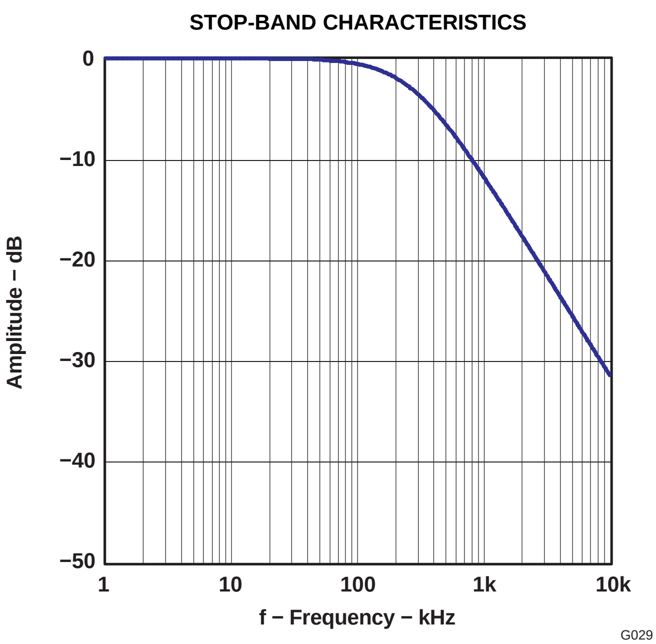


Figure 29.

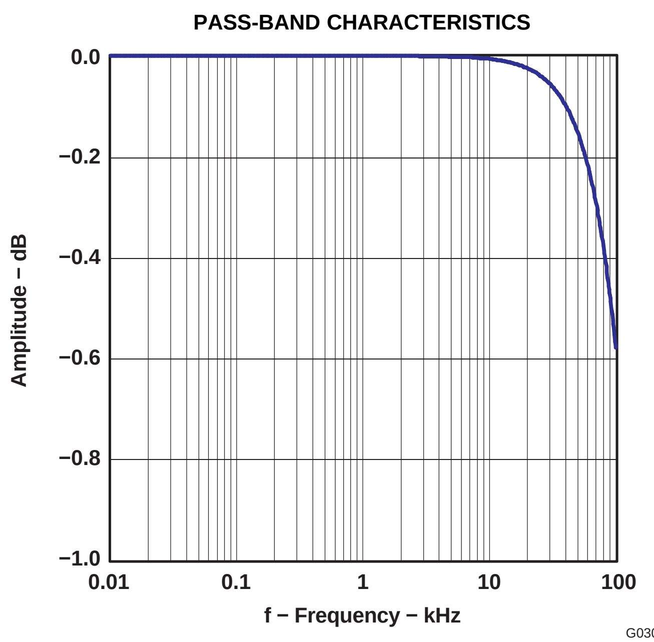


Figure 30.

USB INTERFACE

Control data and audio data are transferred to the PCM2900/2902 via D+ (pin 1) and D– (pin 2). All data to/from the PCM2900/2902 is transferred at full speed. The device descriptor contains the information described in Table 1. The device descriptor can be modified on request; contact a Texas Instruments representative for details.

Table 1. Device Description

USB revision	1.1 compliant
Device class	0x00 (device-defined interface level)
Device subclass	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for end-point 0	8 bytes
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x2900 / 0x2902 (default value, can be modified)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	String #1 (see Table 3)
Product strings	String #2 (see Table 3)
Serial number	Not supported

The configuration descriptor contains the information described in Table 2. The configuration descriptor can be modified on request; contact a Texas Instruments representative for details.

Table 2. Configuration Descriptor

Interface	Four interfaces
Power attribute	0x80 (Bus powered, no remote wakeup)
Max power	0x32 (100 mA. Default value, can be modified)

The string descriptor contains the information described in Table 3. The string descriptor can be modified on request; contact a Texas Instruments representative for details.

Table 3. String Descriptor

#0	0x0409
#1	Burr-Brown from TI (default value, can be modified)
#2	USB audio codec (default value, can be modified)

DEVICE CONFIGURATION

Figure 31 illustrates the USB audio function topology. The PCM2900/2902 has four interfaces. Each interface is constructed by alternative settings.

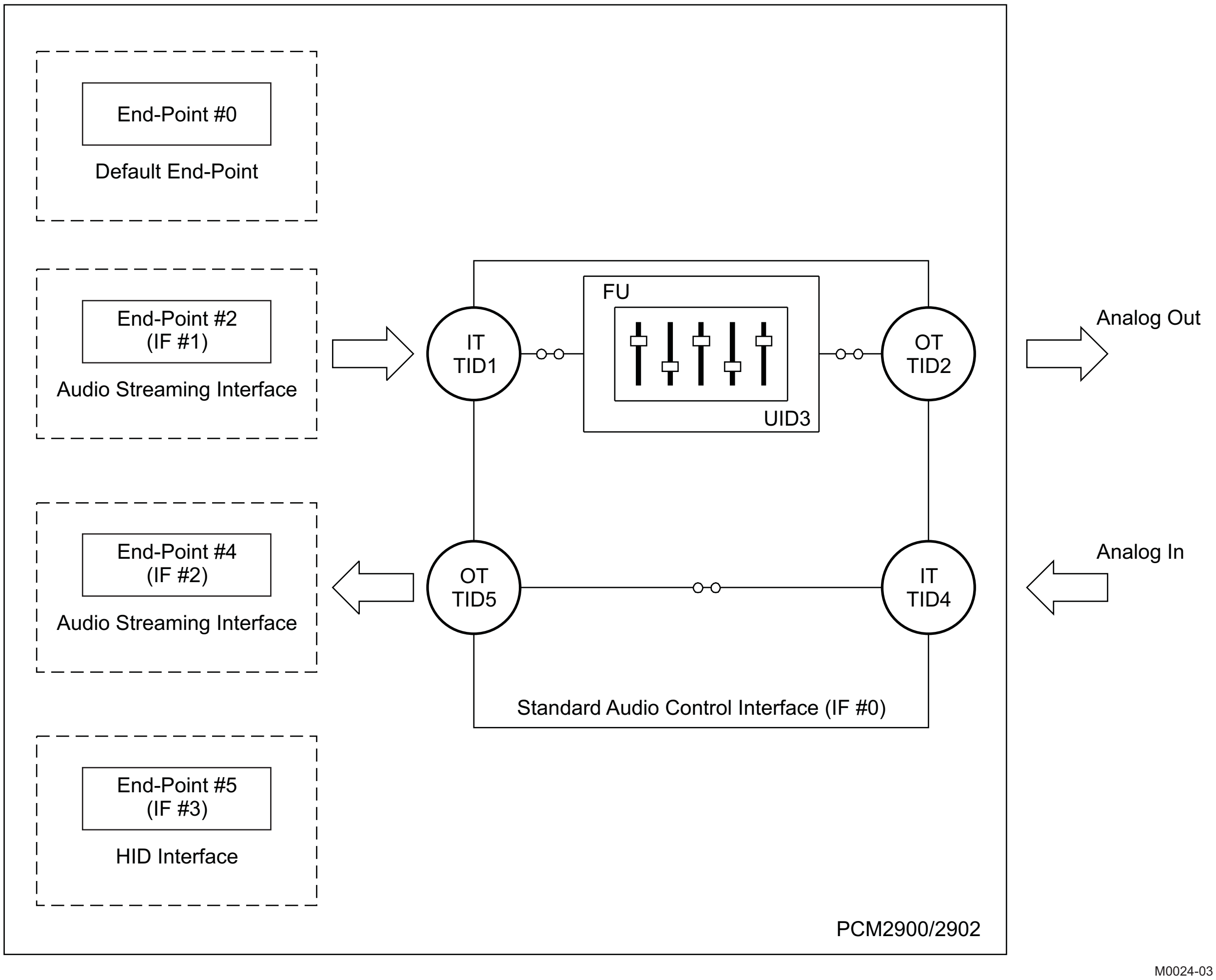


Figure 31. USB Audio Function Topology

Interface #0

Interface #0 is defined as the control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. A terminal constructs the audio control interface. The PCM2900/2902 has five terminals as follows:

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator
- Input terminal (IT #4) for audio analog input
- Output terminal (OT #5) for isochronous-in stream

Input terminal #1 is defined as USB stream (terminal type 0x0101). Input terminal #1 can accept 2-channel audio streams constructed by left and right channels. Output terminal #2 is defined as a speaker (terminal type 0x0301). Input terminal #4 is defined as a microphone (terminal type 0x0201). Output terminal #5 is defined as a USB stream (terminal type 0x0101). Output terminal #5 can generate 2-channel audio streams constructed by left and right channels. Feature unit #3 supports the following sound control features.

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio class specific request from 0 dB to -64 dB in 1-dB steps. Changes are made by incrementing or decrementing by one step (1 dB) for every $1/f_S$ time interval until the volume level has reached the requested value. Each channel can be set for different values. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by audio class specific request. A master mute control request is acceptable. A request to an individual channel is stalled and ignored.

Interface #1

Interface #1 is the audio streaming data-out interface. Interface #1 has the following seven alternative settings. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
02	16 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
03	8 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
04	8 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
05	8 bit	Stereo	Offset binary (PCM8)	Adaptive	32, 44.1, 48
06	8 bit	Mono	Offset binary (PCM8)	Adaptive	32, 44.1, 48

Interface #2

Interface #2 is the audio streaming data-in the interface. Interface #2 has the following 19 alternative settings. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Asynchronous	48
02	16 bit	Mono	2s complement (PCM)	Asynchronous	48
03	16 bit	Stereo	2s complement (PCM)	Asynchronous	44.1
04	16 bit	Mono	2s complement (PCM)	Asynchronous	44.1
05	16 bit	Stereo	2s complement (PCM)	Asynchronous	32
06	16 bit	Mono	2s complement (PCM)	Asynchronous	32
07	16 bit	Stereo	2s complement (PCM)	Asynchronous	22.05
08	16 bit	Mono	2s complement (PCM)	Asynchronous	22.05
09	16 bit	Stereo	2s complement (PCM)	Asynchronous	16
0A	16 bit	Mono	2s complement (PCM)	Asynchronous	16
0B	8 bit	Stereo	2s complement (PCM)	Asynchronous	16
0C	8 bit	Mono	2s complement (PCM)	Asynchronous	16
0D	8 bit	Stereo	2s complement (PCM)	Asynchronous	8
0E	8 bit	Mono	2s complement (PCM)	Asynchronous	8
0F	16 bit	Stereo	2s complement (PCM)	Synchronous	11.025
10	16 bit	Mono	2s complement (PCM)	Synchronous	11.025
11	8 bit	Stereo	2s complement (PCM)	Synchronous	11.025
12	8 bit	Mono	2s complement (PCM)	Synchronous	11.025

Interface #3

Interface #3 is the interrupt data-in interface. Alternative setting #0 is the only possible setting for interface #3. Interface #3 constructs the HID consumer control device and reports the following three key statuses.

- Mute (0xE209)
- Volume up (0xE909)
- Volume down (0xEA09)

End-Points

The PCM2900/2902 has the following four end-points.

- Control end-point (EP #0)
- Isochronous-out audio data stream end-point (EP #2)
- Isochronous-in audio data stream end-point (EP #4)
- HID end-point (EP #5)

The control end-point is a default end-point. The control end-point is used to control all functions of the PCM2900/2902 by the standard USB request and USB audio class specific request from the host. The isochronous-out audio data stream end-point is an audio sink end-point, which receives the PCM audio data. The isochronous-out audio data stream end-point accepts the adaptive transfer mode. The isochronous-in audio data stream end-point is an audio source end-point, which transmits the PCM audio data. The isochronous-in audio data stream end-point uses asynchronous transfer mode. The HID end-point is an interrupt-in end-point. HID end-point reports HID0, HID1, and HID2 pin status every 32 ms.

The human interface device (HID) pins are defined as consumer control devices. The HID function is designed as an independent end-point from both isochronous-in and -out end-points. This means that the result of affection for the HID operation depends on the host software. Typically, the HID function is affected for the primary audio-out device.

Clock and Reset

The PCM2900/2902 requires a 12-MHz (±500 ppm) clock for the USB and audio function, which can be generated by a built-in crystal oscillator with a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to XTI (pin 21) and XTO (pin 20) with one high (1-MΩ) resistor and two small capacitors, the capacitance of which depends on the load capacitance of the crystal resonator. The external clock can be supplied from XTI (pin 21). If the external clock is supplied, XTO (pin 20) must be left open. Because of no clock-disabling signal, it is not recommended to use the external clock supply. $\overline{\text{SSPND}}$ (pin 28) is unable to use clock disabling.

The PCM2900/2902 has an internal power-on reset circuit, which works automatically when V_{BUS} (pin 3) exceeds 2.5 V typical (2.7 V–2.2 V), and about 700 µs is required until internal reset release.

Digital Audio Interface (PCM2902)

The PCM2902 employs both S/PDIF input and output. Isochronous-out data from the host is encoded to the S/PDIF output and the DAC analog output. Input data is selected as either S/PDIF or ADC analog input. When the device detects an S/PDIF input and successfully locks the received data, the isochronous-in transfer data source is automatically selected from S/PDIF itself; otherwise, the data source is selected to ADC analog input.

Supported Input Data (PCM2902)

The following data formats are accepted by the S/PDIF input and output. All other data formats are unable to use S/PDIF.

- 48-kHz 16-bit stereo
- 44.1-kHz 16-bit stereo
- 32-kHz 16-bit stereo

Mismatch between input data format and host command may cause unexpected results except in the following conditions.

- Record monaural format from stereo data input at the same data rate
- Record 8-bit format from 16-bit data input at the same data rate

A combination between the above conditions is not accepted.

For the playback, all possible data rate source is converted to 16-bit stereo format at the same source data rate.

Channel Status Information (PCM2902)

The channel status information is fixed as consumer application, PCM mode, copyright, and digital/digital converter. All other bits are fixed as 0s except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management (PCM2902)

Isochronous-in data is affected by the serial copy management system (SCMS). Where receiving digital audio data that is indicated as original data in the control bit, input digital audio data transfers to the host. If the data is indicated as first generation or higher, transferred data is selected to analog input.

Digital audio data output is always encoded as original with SCMS control.

The implementation of this feature is an option for the customer. Note that it is the user's responsibility whether they implement this feature in their product or not.

INTERFACE SEQUENCE

Power On, Attach, and Playback Sequence

The PCM2900/2902 is ready for setup when the reset sequence has finished and the USB bus is attached. After connection has been established by setup, the PCM2900/2902 is ready to accept USB audio data. While waiting, the audio data (idle state) and analog output are set to bipolar zero (BPZ).

When receiving the audio data, the PCM2900/2902 stores the first audio packet, which contained 1-ms audio data, into the internal storage buffer. The PCM2900/2902 starts playing the audio data when detecting the following start of frame (SOF) packet.

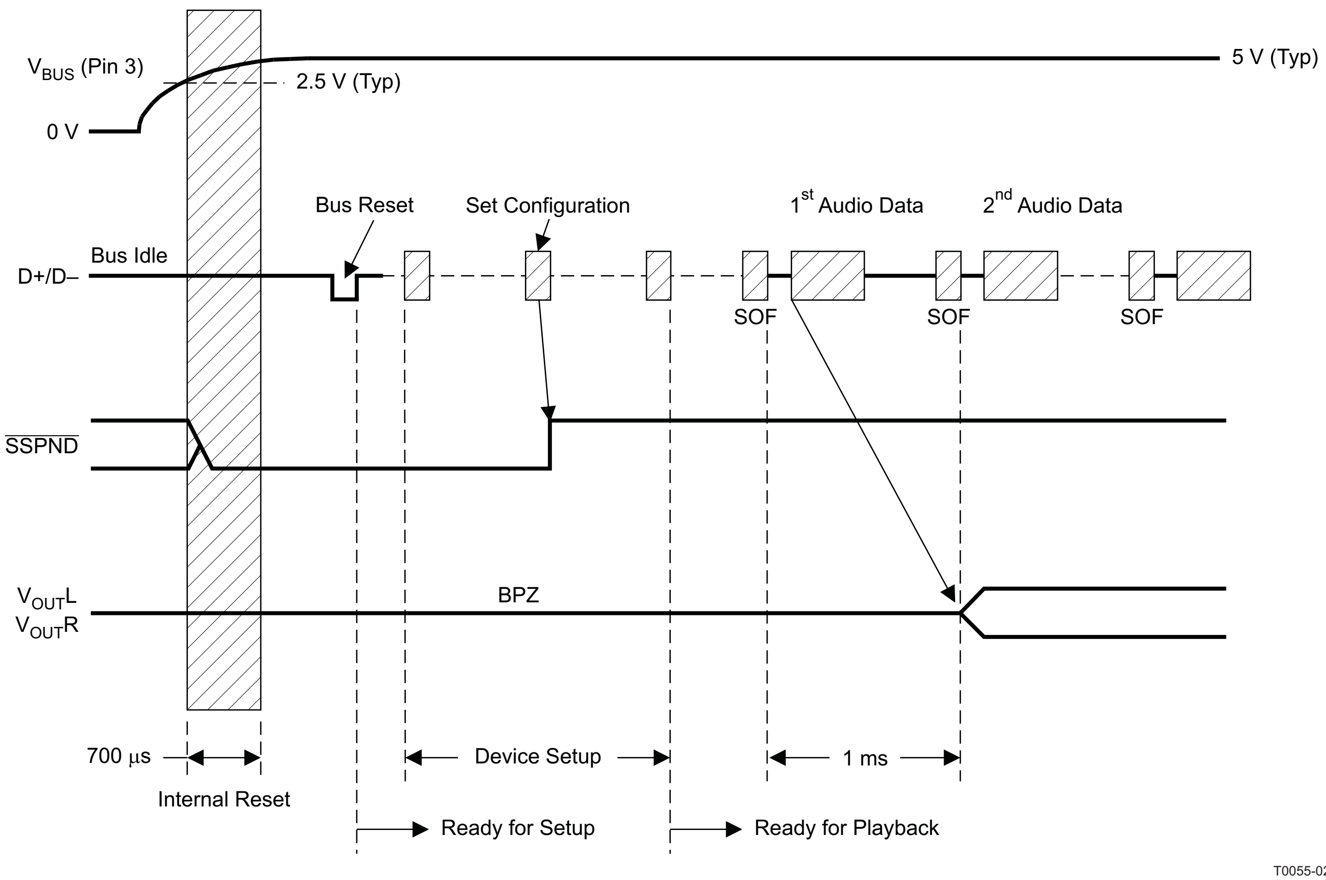


Figure 32. Initial Sequence

Play, Stop, and Detach Sequence

When the host finishes or aborts the playback, the PCM2900/2902 stops playing after the last audio data has played.

Record Sequence

The PCM2900/2902 starts the audio capture into the internal memory after receiving the SET_INTERFACE command.

Suspend and Resume Sequence

The PCM2900/2902 enters the suspend state after it sees a constant idle state on the USB bus, approximately 5 ms. While the PCM2900/2902 enters the suspend state, $\overline{SSPND}$ flag (pin 28) is asserted. The PCM2900/2902 wakes up immediately when detecting the non-idle state on the USB bus.

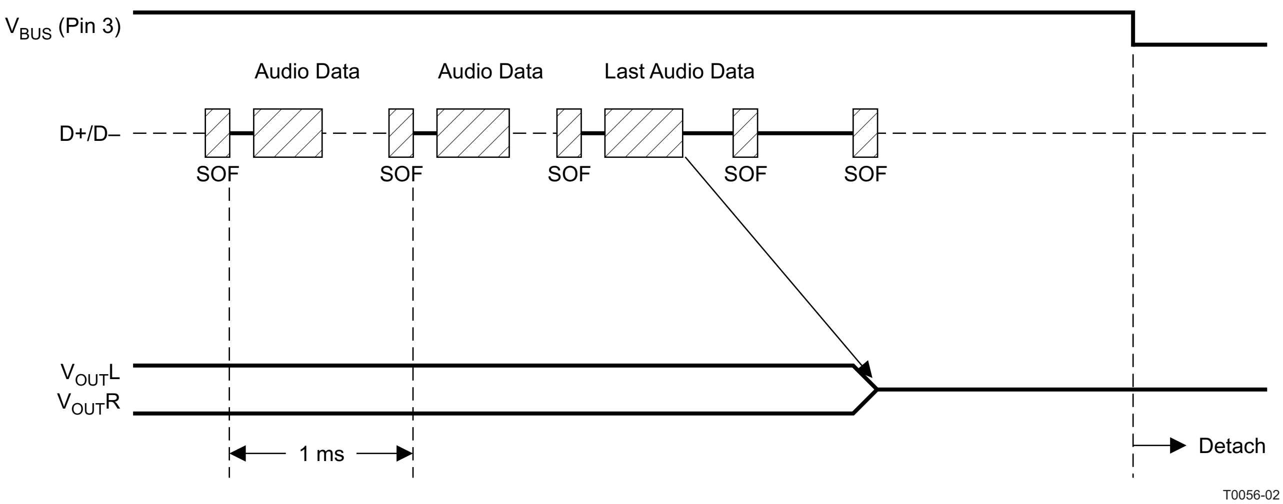


Figure 33. Play, Stop, and Detach

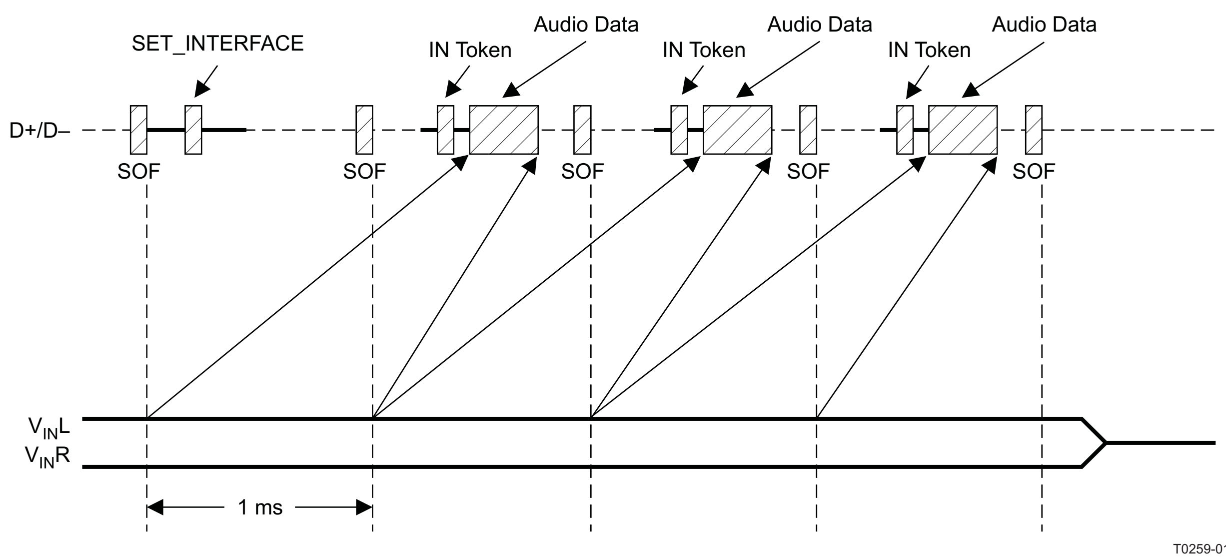


Figure 34. Record Sequence

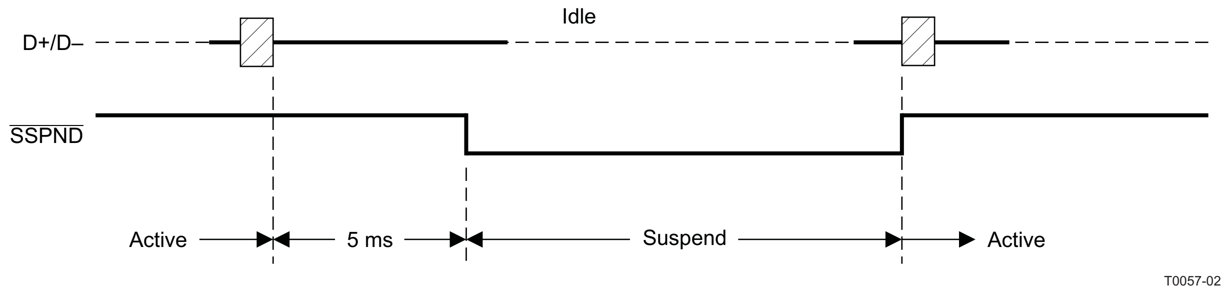
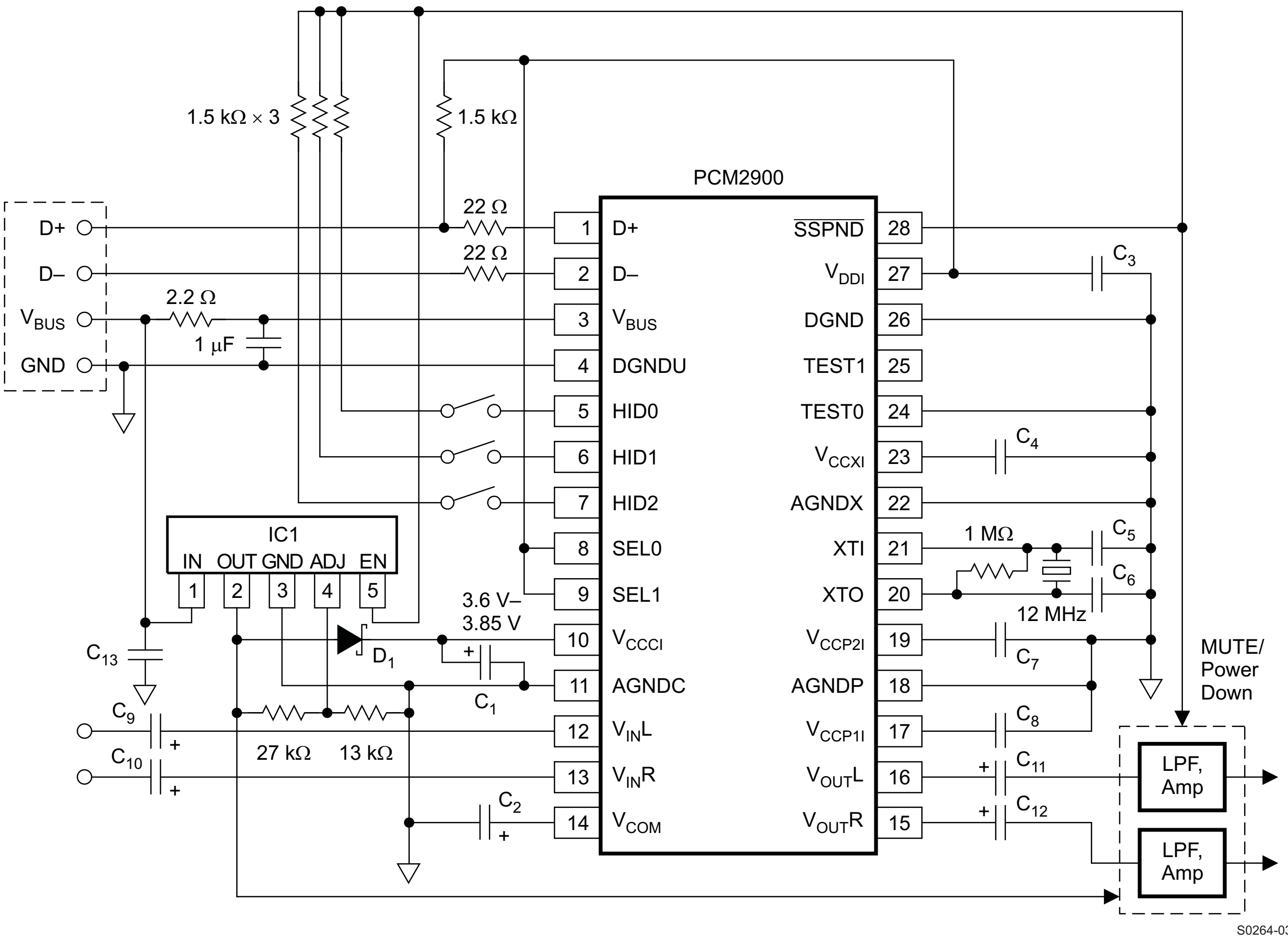


Figure 35. Suspend and Resume

PCM2900 TYPICAL CIRCUIT CONNECTION 1

Figure 36 illustrates a typical circuit connection for a high-performance application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB-compliant product.

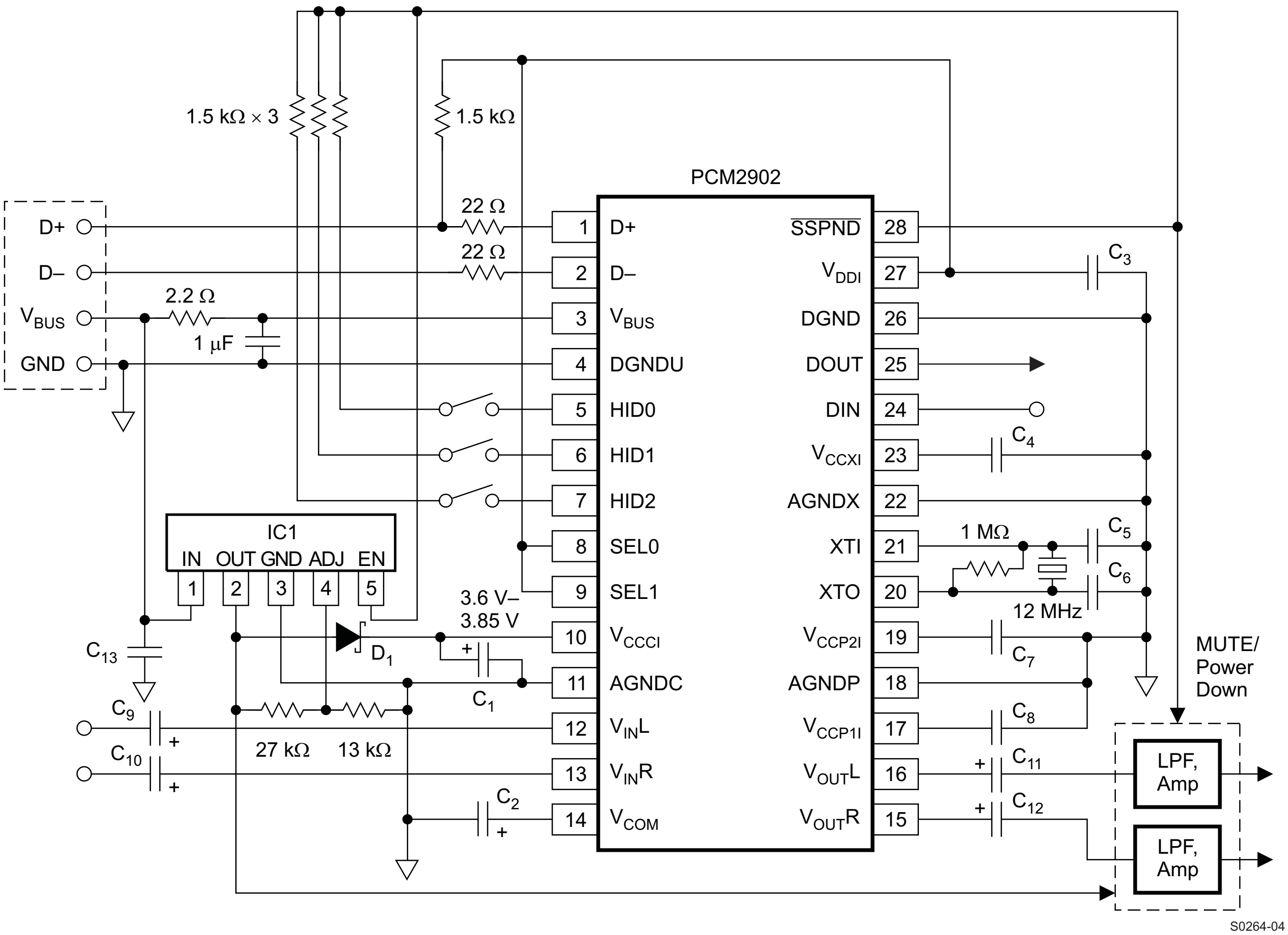


NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8, C_{13}: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
IC1: REG103xA-A (TI) or equivalent. Analog performance may vary depending on IC1.
D_1: Schottky barrier diode ($V_F \le 350$ mV at 10 mA, $I_R \le 2$ µA at 4 V)

Figure 36. Bus-Powered Configuration for High-Performance Application

PCM2902 TYPICAL CIRCUIT CONNECTION 1

Figure 37 illustrates a typical circuit connection for a high-performance application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB-compliant product.

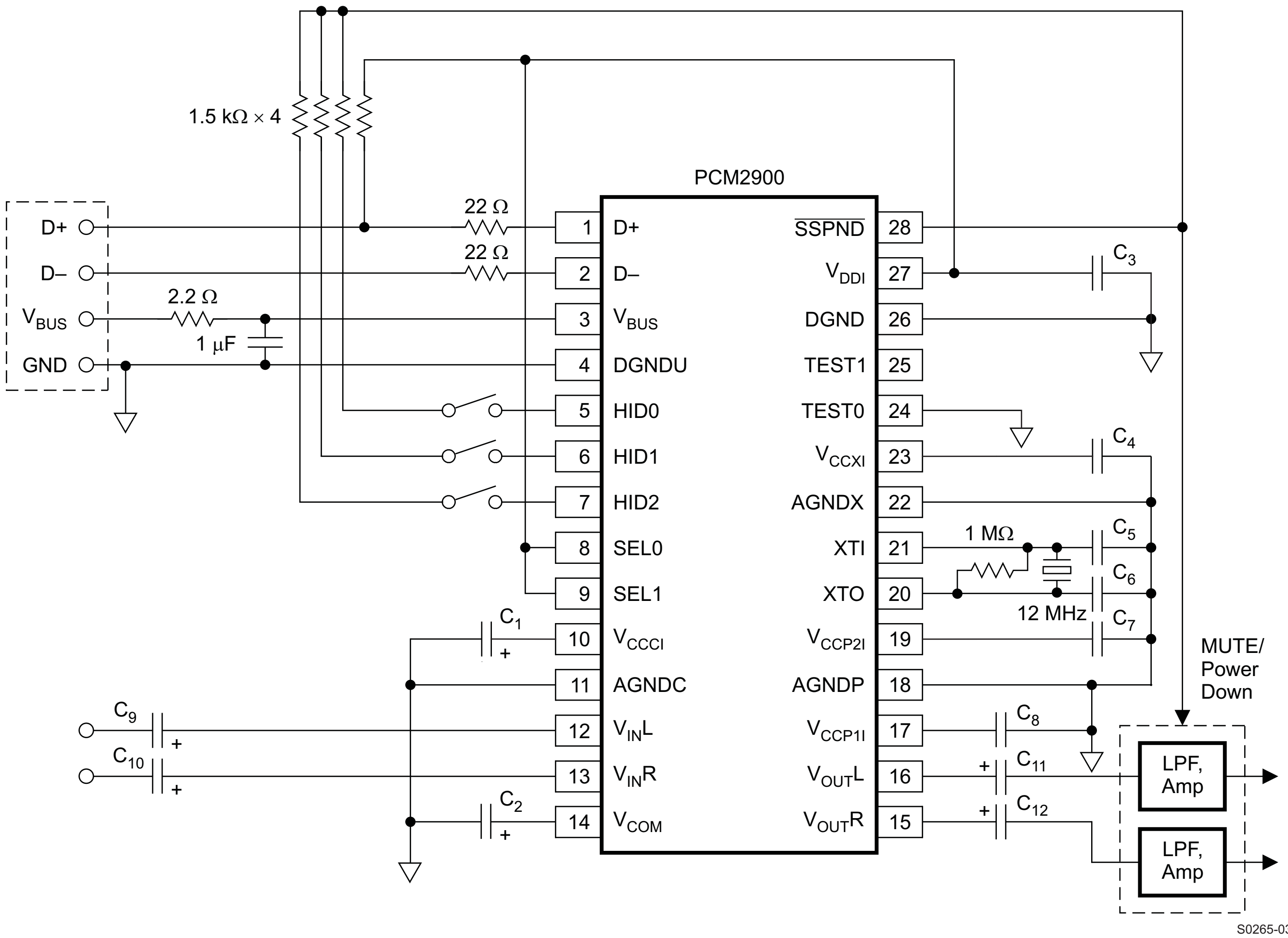


NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8, C_{13}: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
IC1: REG103xA-A (TI) or equivalent. Analog performance may vary depending on IC1.
D_1: Schottky barrier diode ($V_F \leq 350$ mV at 10 mA, $I_R \leq 2$ µA at 4 V)

Figure 37. Bus-Powered Configuration for High-Performance Application

PCM2900 TYPICAL CIRCUIT CONNECTION 2

Figure 38 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB-compliant product.

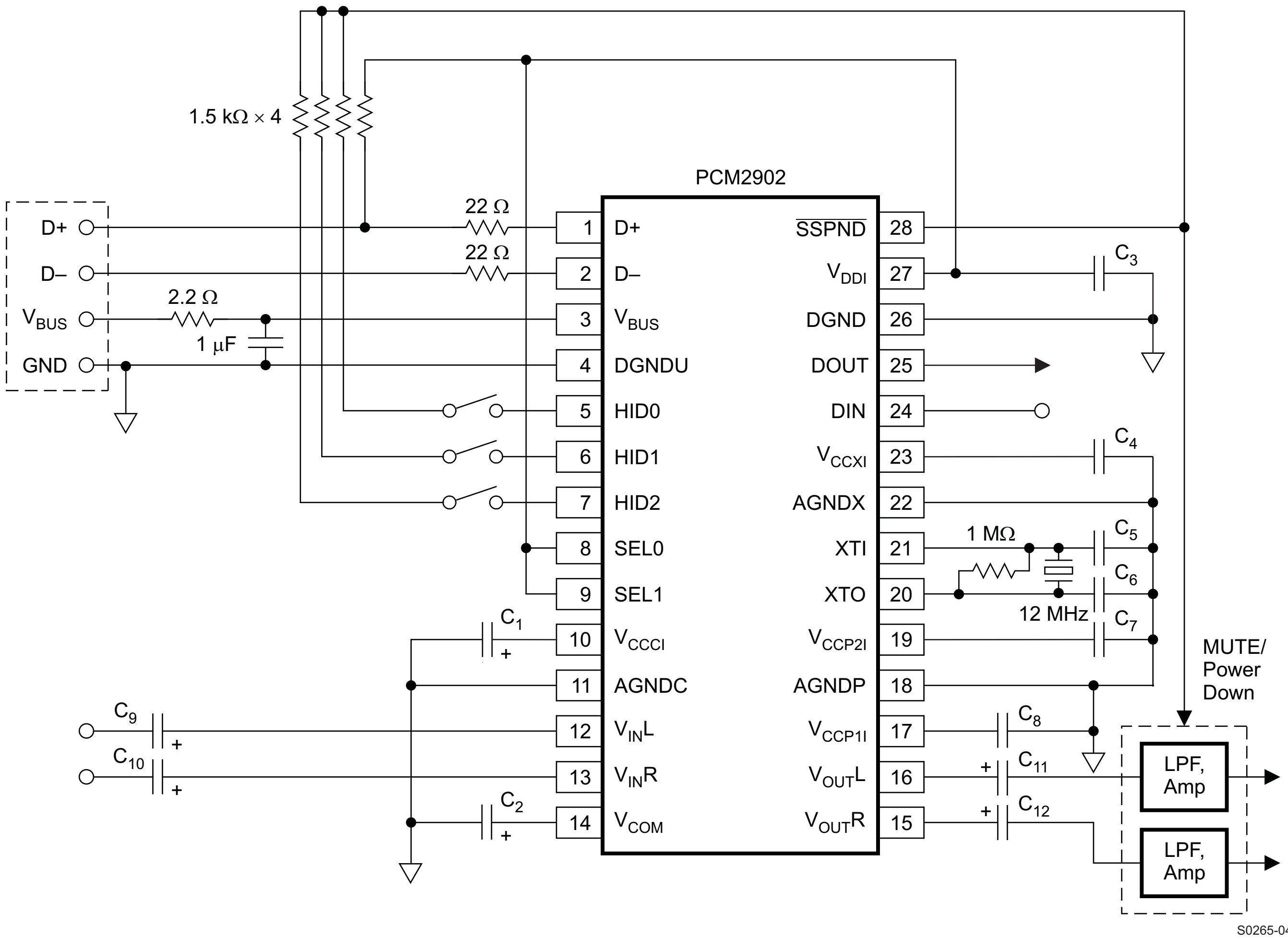


NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
In this case, the analog performance of the A/D converter may be degraded.

Figure 38. Bus-Powered Configuration

PCM2902 TYPICAL CIRCUIT CONNECTION 2

Figure 39 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB-compliant product.



NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
In this case, the analog performance of the A/D converter may be degraded.

Figure 39. Bus-Powered Configuration

APPLICATION INFORMATION

OPERATING ENVIRONMENT

For current information on the PCM2900/2902 operating environment, see the *Updated Operating Environments for PCM270X, PCM290X Applications* application report, SLAA374.

REVISION HISTORY

Changes from Original (March 2002) to Revision A	Page
• Changed the status from Product Preview to Production Provided the full data sheet..	1

Changes from Revision A (May 2002) to Revision B	Page
• Changed the description.	1
• Changed Interface #2 to include lines 0F, 10, 11, and 12.	22
• Added Channel Status Information (PCM2902).	24
• Deleted Note: The circuit illustrated above is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product. From Figure 36, Figure 37, and Figure 38	27

Changes from Revision B (June 2004) to Revision C	Page
• Changed Figure 36, Figure 37, and Figure 38	27

Changes from Revision C (March 2007) to Revision D	Page
• Deleted operating environment information from data sheet and added reference to application report	31

Changes from Revision D (November 2007) to Revision E	Page
• Changed the Packageing Ordering Information Table to correct the Specified Temperature Range From 25°C to –25°C for the PCM2900 and PCM2902.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM2900E	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2900E/2K	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2900E/2KG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2900EG4	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2902E	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2902E/2K	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2902E/2KG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCM2902EG4	ACTIVE	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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